



Design and Analysis of Parallel Prefix Adder for Reverse Converter

Kavya S^a & Amala M^b

^aPG Student, Dept. of Electronics and Communication, C Byregowda Institute of Technology, Kolar, India.

^bAsst. Prof, Dept. of Electronics and Communication, C Byregowda Institute of Technology, Kolar, India.

ABSTRACT

This paper presents an efficient parallel prefix adder for reverse convertor. Residue number system is a non-weighted integer number representation system which is capable of supporting parallel, carry free and high speed arithmetic operations. Forward Convertor, modulo arithmetic unit and Reverse convertor are the main parts of the Residue Number System [1]. Reverse Convertor that is residue to binary convertor is complex structure and also it is based on the regular and modular parallel prefix adder. Nowadays the parallel prefix adders are not used even though it provides significant delay reduction and high speed operation because of higher power consumption. The novel specific hybrid parallel prefix based adder components that compensate the delay and power consumption in the existing system are applied. Different parallel adder structures are analyzed among that Brent-Kung prefix network is used for the parallel prefix addition because of the minimum fan-out.

Keywords - Digital arithmetic, parallel-prefix adder, residue number system (RNS), reverse converter.

1. INTRODUCTION

Parallel Prefix based Adder (PPA) [4] is extremely effective in today's era of innovation in light of its execution in Very Large Scale Integration (VLSI) chips. The VLSI chips depend comprehensively on fast arithmetic computation. These fast addition techniques are essential in enhancing arithmetic unit performance because other arithmetic operations for example, multiplication and division are based on addition; subsequently their delay heavily relies on the addition. Due to the area, power consumption and delay we are introducing the parallel prefix adder XOR /OR and to design fast reverse converters. To improve the performance of existing method we are implementing a method called hybrid parallel prefix excess one adder. Using this adder the area, delay and power consumption are definitely improved. Finally the power has been gained nearly 35% in parallel prefix adder and by using hybrid parallel prefix excess one adder the power is improved nearly 42%.

1.1 Statement of the Problem

Execution of residue number system reverse converters built up on well-known traditional and modular parallel prefix based adders controls a huge delay reduction and area and time enhancements, with the cost of high power consumption. Consequently designer keeps the utilization of parallel-prefix based adders to accomplish fast speed reverse converters in all digital systems. To defeat the high power consumption issue, unique hybrid parallel-prefix based adder mechanisms that give better trade-off between delay and power consumption are displayed to outline reverse converters.

2. BK PREFIX NETWORK

The parallel prefix adders are more flexible and they are used to speed up the binary additions. Parallel prefix adders are getting from Carry Look Ahead structure. We use tree structure for increase the speed of arithmetic operation. Parallel prefix adders are fastest adders and these adders are used for high performance arithmetic circuits in VLSI. The construction of parallel prefix adder involves three stages.

2.1 Pre-Processing Unit

The preprocessing stage registers the carry-generate bits G_i , the carry-propagate bits P_i , and the half-sum bits H_i , for every i , $0 \leq i \leq n-1$. Where, '+' and ' \oplus ' denote logical AND, OR, and exclusive-OR, respectively.

Carry generation bits $\Rightarrow G_i = A_i \cdot B_i$

Carry propagate bits $\Rightarrow P_i = A_i + B_i$

Half sum bits $\Rightarrow H_i = A_i \oplus B_i$

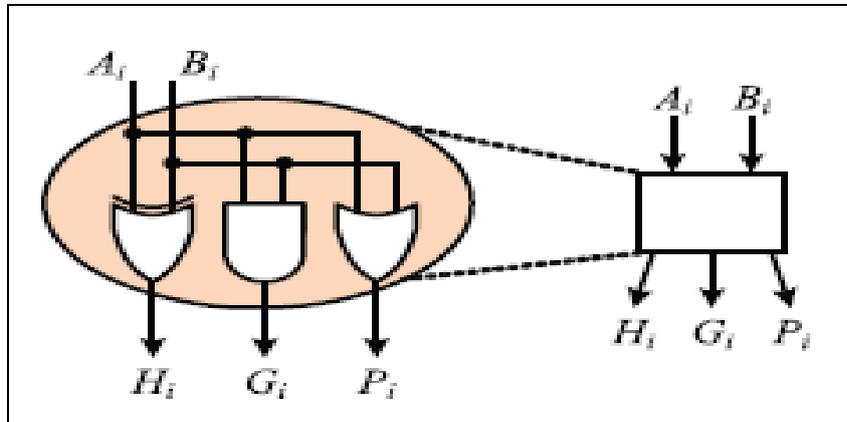


Fig 1: Preprocessing Unit.

2.2 Carry Computation Unit

Second stage of the adder is called as carry computation unit, which computes the carry signals C_i , for $0 \leq i \leq n - 1$ utilizing the carry generate bit G_i and carry propagate bit P_i . The third stage computes the sum bits.

$S_i = H_i \oplus C_{i-1}$

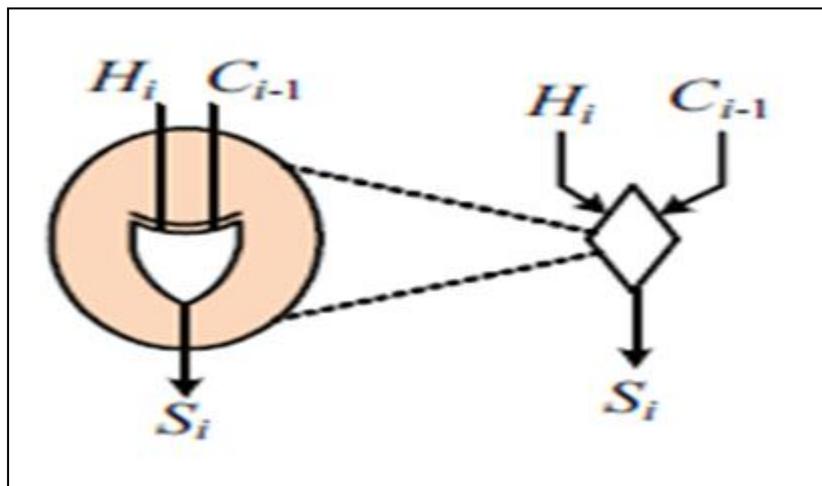


Fig 2: Carry Computation Unit.

Computation of carry signal is transformed into a parallel prefix problem using the "o" operator, which will associate the pairs of generate and propagate signals and it is defined as,

$$(G, P) \circ (G', P') = (G + P \cdot G', P \cdot P')$$

In a series of associations with the successive generate and propagate pairs $(G; P)$ and it can be represented as

$$(G_{k:j} : P_{k:j}) = (G_k, P_k) \circ (G_{k-1}, P_{k-1}) \circ \dots \circ (G_j, P_j) \quad \text{Where, } k > j$$

2.3 Black Ball

Parallel prefix adders are constructed out of fundamental carry operators denoted by ϕ as follows:

$$(G'', P'') \phi (G', P') = (G'' + G' \cdot P'', P' \cdot P''),$$

where P'' and P' indicate the propagations, G'' and G' indicate the generations.

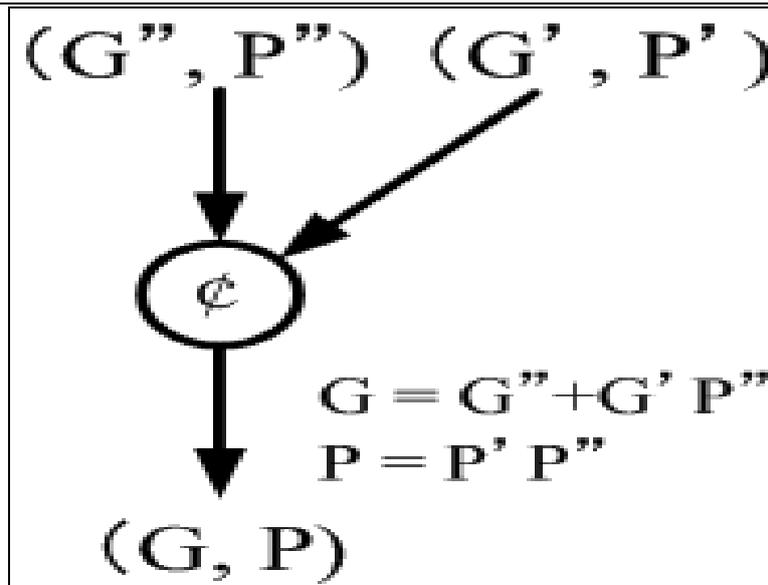


Fig 3: Carry Operator.

A parallel prefix adder can be represented as a parallel prefix graph consisting of carry operator nodes.

3. EXISTING DESIGN

HRPX STRUCTURE: A conventional parallel-prefix based adder with the coveted prefix structure can be utilized to perform the first part of the addition, for which the identical bits of the operands are completely variable, and a RCA with abbreviated logic to do the second part. The proposed Hybrid Regular Parallel-prefix XOR/OR (HRPX) [14] adder segment to perform the $(4n + 1)$ -bit addition of [10, CPA4] for $n = 4$. It ought to be analyzed that because of the architecture of reverse converter, the carry output of the XNOR/OR chain is not required and can be disregarded. Second, the modulo $2n - 1$ addition is a vital operation in the reverse conversion for most moduli sets. The customary CPA with End Around Carry (EAC) is a matter of course a modulo $2n - 1$ adder with double representation of zero, however, in reverse converters a solitary representation of zero is needed.

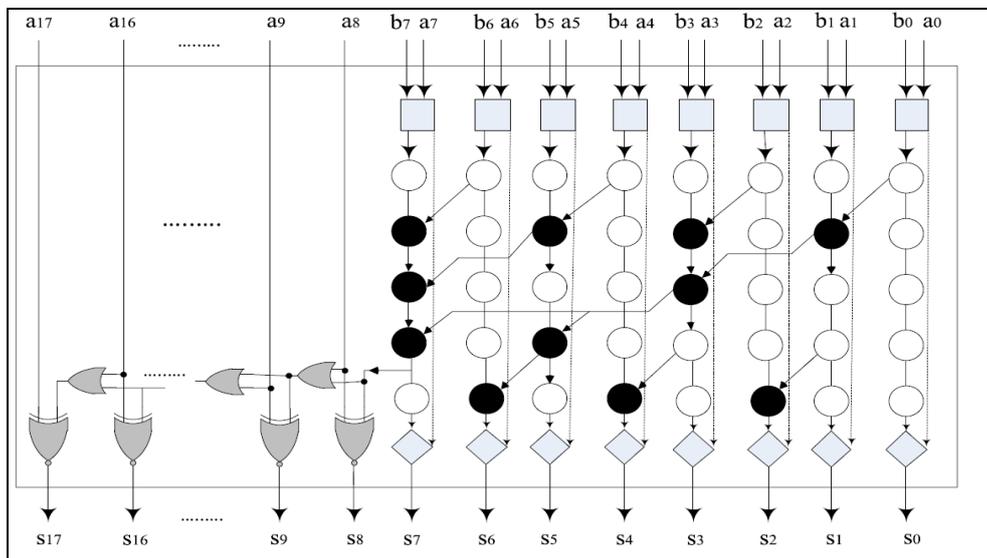


Fig 4: HRPX Structure with BK Prefix Network.

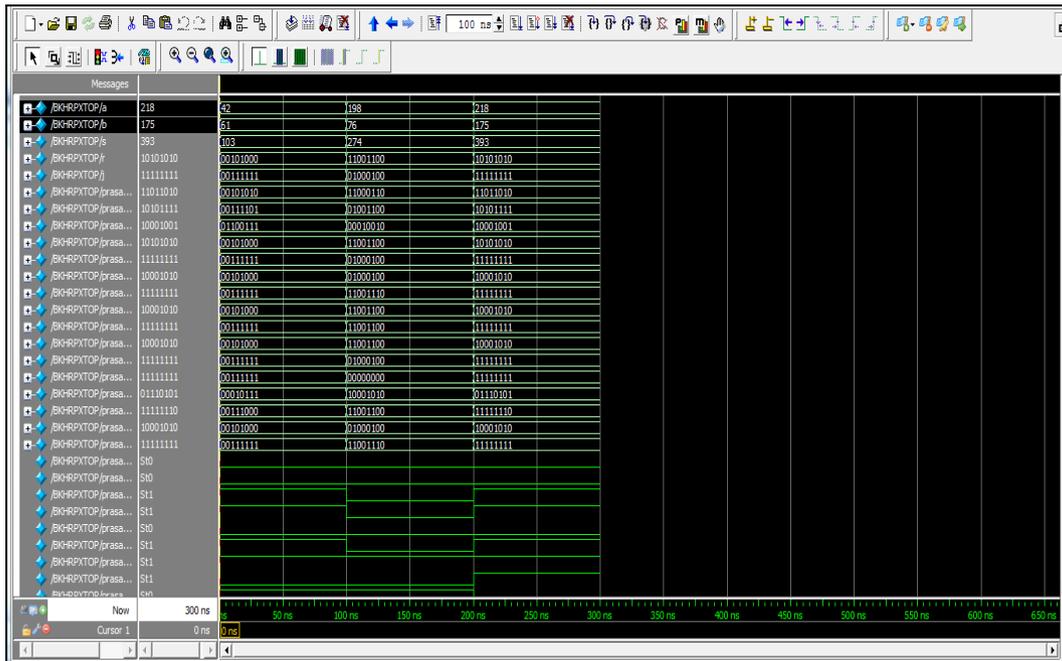


Fig 5: Results of BK with HRPX.

4. PROPOSED DESIGN

HMPE STRUCTURE: A moduli $2n - 1$ adder with double representation of zero, yet in reverse converters a solitary representation of zero is needed. Along these lines, a one detector circuit must be utilized to correct the outcome, which forces an extra delay. Nonetheless, there is a binary-to-excess-one converter (BEC) [12], which can be adjusted to alter the double-representation of zero issue. The principle purpose behind the high power consumption and area overhead of these adders is the recursive impact of generating and propagating signals at every prefix level. A streamlined methodology is proposed in, which utilizes an additional prefix level to include the output carry. Nonetheless, this system experiences from high fan-out, which can make it usable just for small width operands. In any case, we could address this issue by eliminating the extra prefix level and utilizing a modified excess-one unit instead. Rather than the BEC, this modified unit has the capacity to perform a conditional increment in light of control signals as shown in Fig 6, and the resulted hybrid modular parallel-prefix excess-one (HMPE) adder is delineated in Fig 7.

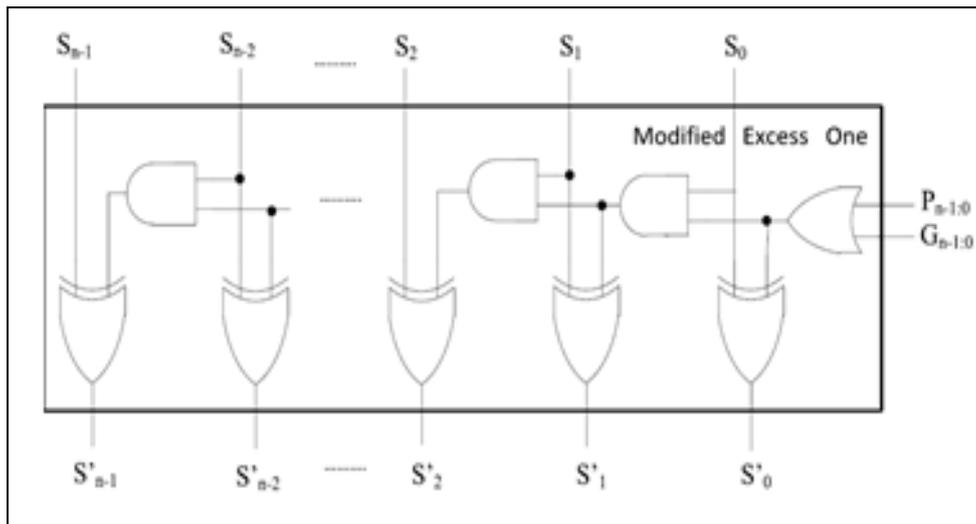


Fig 6: Modified Excess One Unit.

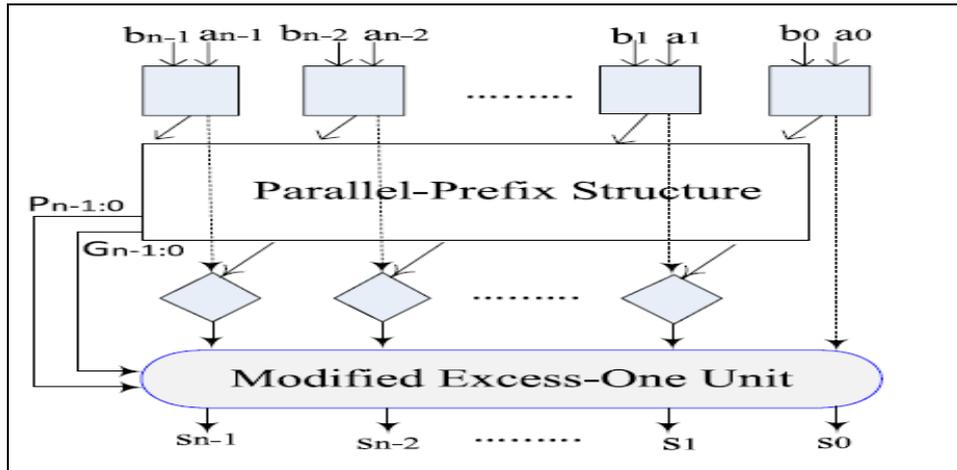


Fig 7: HMPE Structure.

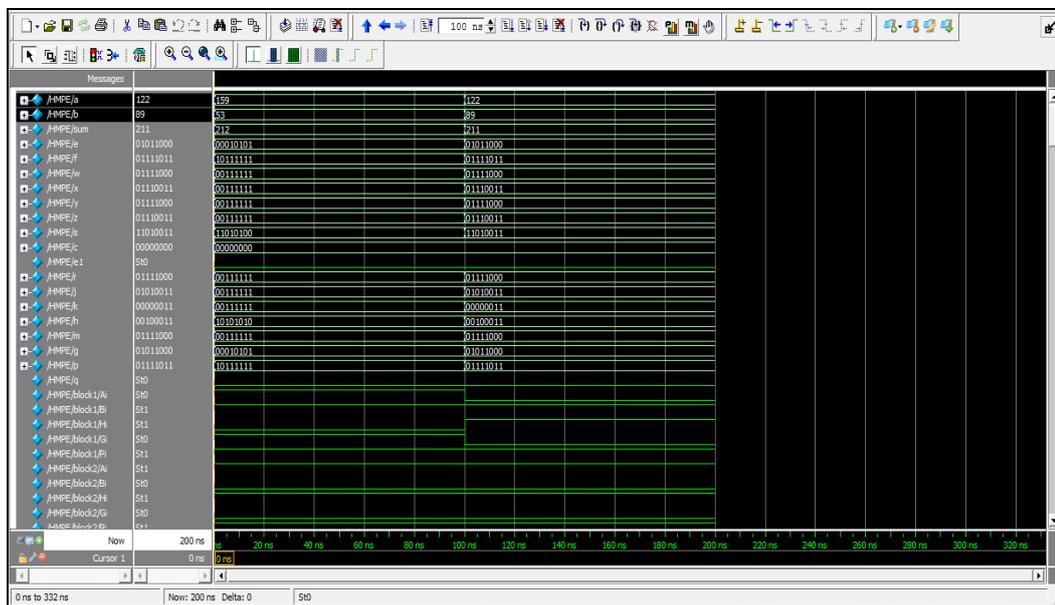


Fig 8: Results of BK with HMPE.

| Structure | Area | Delay |
|---------------------|------|----------|
| HMPE and HRPX KS | 363 | 24.303ns |
| HMPE and HRPX LF | 330 | 24.604ns |
| MPE and HRPX BK | 339 | 24.578ns |
| Ripple Carry Adder | 264 | 26.612ns |
| Fully Prefix Adder | 639 | 17.230ns |

Table 1: Comparison Table of Parallel Prefix Adders.

5. CONCLUSION AND FUTURE WORK

Adders are the functional blocks which are by and large intended for faster operation. In any case, Power dissipation cannot have less priority any longer. Using parallel prefix adders is a decent design practice for trading-off between speed, power dissipation and area. It is seen in the literature that it is not possible to have more speed anymore from the designed circuits in the execution perspective. However, the design space is extremely incomprehensible and there always exists potential outcomes for improvements. In this thesis we designed a hybrid modular parallel prefix adder to show the delay and area reduction.

This brief shows a technique that can be applied to the vast of the current reverse convertor architectures to upgrade their performance and adjust the cost to the application specifications. Moreover, in order to provide the required trade-offs between performance and cost, new parallel-prefix based adder components were introduced. These components are specially designed for reverse convertors. Implementation results show that the reverse convertors based on the suggested components considerably improve the speed when compared with original convertors, which do not use any parallel-prefix adder.

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