International Journal for Ignited Minds (IJIMIINDS)

Design of Low Power Double-Tail Dynamic Comparator Using Sleep Methods

Shruthi S[a] & Prof. Ashwini N C[b]

[a]*PG Scholar, Department of E&C, C Byregowda Institute of Technology, Kolar, India.*
[b]*Prof, Department of E&C, C Byregowda Institute of Technology, Kolar, India.*

ABSTRACT

Analog to Digital Converter requires high speed, area efficient and low power comparators is forcing towards the use of Dynamic comparator. Higher power consumption will reduce the life time of the battery. The demand for long battery lifetime in applications poses the requirement for designing ultra-low power Dynamic comparators. In this paper an analysis on the power of single-tail and double-tail comparators are presented. Based on analysis a new Dynamic comparator is modified using Sleep methods for leakage power reduction even in small supply voltages like sleep, stack, sleepy-stack etc. Transient simulation results in a 250nm Tanner EDA tool confirm the analysis result. It is shown that among the proposed dynamic comparators, stack approach-Dynamic comparator reduces more power consumption.

Keywords *- Analog to digital conversion (ADC), CMOS, Dynamic comparator, Double Tail Comparator, Sleep Methods, Tanner EDA.*

1. INTRODUCTION

COMPARATOR is one of the basic building blocks in most analog-to-digital converters (ADCs). Many high speed ADCs, such as SAR ADCs, require low-power, high-speed comparators with small-chip area. High-speed comparators in ultra deep sub-micrometer CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes. Hence, designing comparators with high speed is more challenging when the supply voltage is smaller [1]. Present requirement of low power for digital VLSI circuit is increasing day by day. The demand of high battery life and environmental concern of power dissipation by electronics design creates a global consensus for low power VLSI design. Besides, low-voltage operation results in small common-mode input range, which is important in many ADC architectures, such as SAR ADCs. Many techniques, such as supply boosting methods [2], [3], techniques employing current-mode design [6], body-driven transistors [4], [5] and those using dual-oxide processes, which can handle greater supply voltages have been developed to meet the low-voltage design challenges. Boosting and bootstrapping are techniques based on adding the supply, reference, or clock voltage to address input-range and switching problems. These techniques are successful in producing a desired result, but they introduce reliability issues especially in UDSM CMOS technologies.

1.1. Statement of the Problem

Low power design means design that dissipates minimum static and dynamic power. Every sequential circuit has high static and dynamic power consumption because one input of the circuit is clock. Clock is the signal that switches all the time. In addition, the clock signal tends to be highly loaded. Current experiment and studies proves that in digital VLSI circuit, clock signals consume a major portion of the system power. To overcome that, sleep methods [7] are used with the conventional dynamic comparators to achieve low power ADC.

In this paper, an analysis about the power of dynamic comparators has been presented for different comparator architectures. In addition, based on the double-tail structure proposed in [8], a new dynamic comparator is presented, which do not require boosted voltage or arranging of too many transistors. This can achieve by adding a few minimum-size transistors to the conventional dynamic comparator. This modification also results notably

large in power savings when compared to the conventional double-tail comparator. The remaining of this paper is organized as follows. Section 2 investigates the operation of the existing double - tail comparator is discussed. The proposed comparator is presented in Section 3. Simulation results are addressed in Section 4, followed by conclusions in Section 5 and Future Work in Section 6.

2. CLOCKED REGENERATIVE COMPARATOR

Clocked regenerative comparators called as dynamic comparator have found wide applications in high speed ADCs because they make fast decisions due to positive feedback in the latch. In this section an analysis of single tail and double tail dynamic comparators were presented.

2.1 Existing Double-Tail Dynamic Comparator

Fig 1 [8] briefs the schematic diagram with simulation result of the double-tail comparator. In this structure some more power consumption can be reduced due to the logic adopted in the design and also by adding few transistors to conventional double tail comparators. The operation of this comparator is as follows. During reset phase when CLK = 0, Mtail1 and Mtail2 are off, avoiding static power, M3 and M4 pulls both fn and fp nodes to Vdd, transistors MC1 and MC2 are off. Intermediate transistor, MR1 and MR2 resets bots latch output to ground. During decision making phase when CLK = Vdd, Mtail1 and Mtail2 are on, transistors M3 and M4 turn off. In addition at the beginning of this phase the control transistors are still off. Thus fn and fp starts to discharge with different rates depending on the input voltages. Suppose Vinn > Vinp, fp drops faster than fn. As long as fp continues falling, the corresponding pMos control transistor MC2 starts to turn on, pulling fn node back to the Vdd, so another control transistors remains off allowing fp to be discharged completely.

From the figure below, it is given CLK = Vdd when Vinp > Vinn, Outn discharges to ground with reduced latch regeneration delay and Outp remains at Vdd.

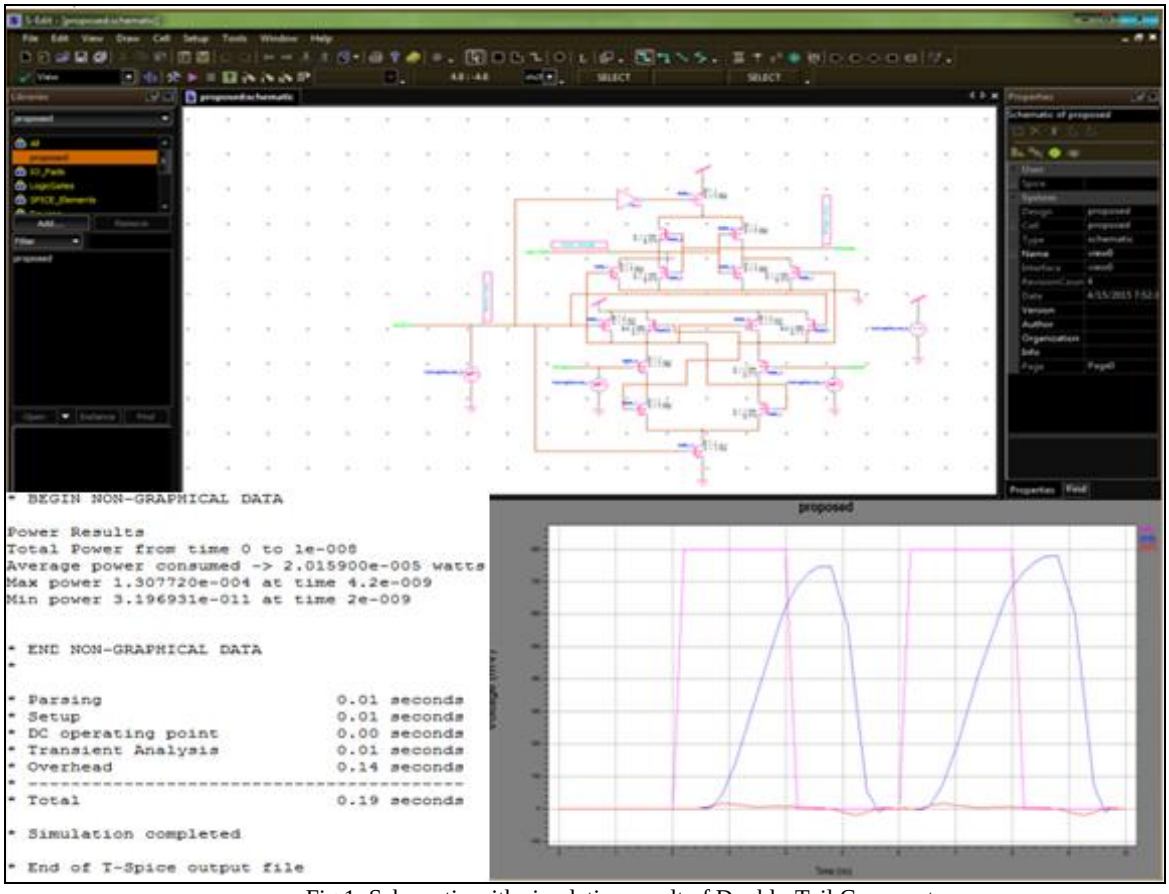

Fig 1: Schematic with simulation result of Double-Tail Comparator.

3. PROPOSED DYNAMIC COMPARATORS WITH SLEEP METHODS

Comparative study of double tail comparators using sleep methods by Using Sleep Transistor Technique, Forced Stacking Technique and Sleepy-stack Technique are described below:

3.1 Using Sleep Transistor Technique

The schematic diagram of the proposed dynamic comparator is shown in the Fig 2. Due to the better performance of double-tail dynamic architecture in low voltage applications, the proposed comparator is designed based on the double-tail structure. Here we can achieve the reduced power consumption of what obtained in previous double-tail comparator by using sleep transistor technique. Static power consumption is a major concern in nanometer technologies [7], [9]. Along with technology scaling down and higher operating speeds of CMOS VLSI circuits, the leakage power is getting enhanced. The power dissipation during standby mode of operation can be significantly reduced by sleep transistor technique. This technique uses additional transistors which are inserted in series between the power supply and pull-up pMOS network and/or between pull-down nMOS network and ground to reduce the standby leakage power. The sleep transistors are turned on when circuit are in active mode and turned off when circuit is in standby mode.

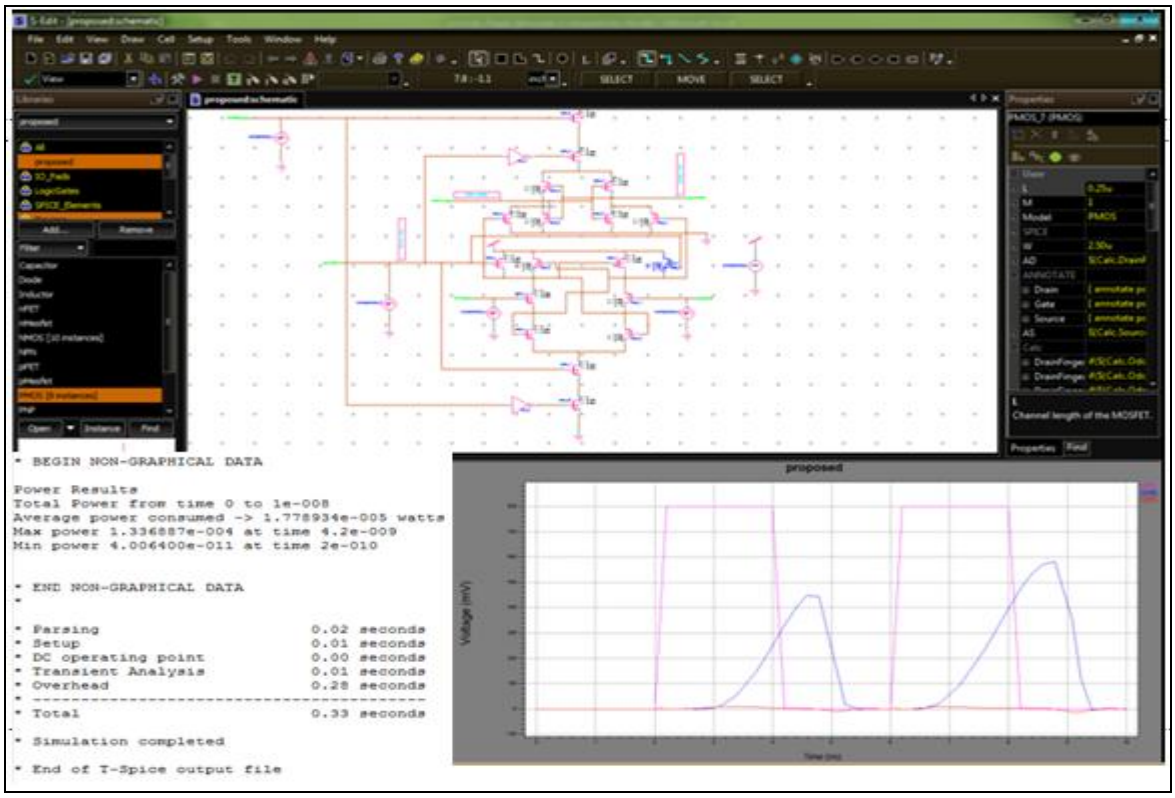

Fig 2: Schematic with simulation result of Proposed Double-Tail Comparator with Sleep Transistor Technique.

3.2 Using Stack Technique

The schematic with simulation result diagram of the proposed double-tail comparator with stack approach is shown in Fig 3. This technique replaces an input (CLOCK) transistor of the ratio W/L=X to two transistors of the ratio W/L=X/2, which are inserted in series between the power supply and pull-up pMOS network and/or between pull-down nMOS network and ground. The forced stack can achieve huge power saving while retaining the logic state. The remaining structure of schematic operates as same of Double-Tail Comparator. The effect of stacking the transistor results in the reduction of subthreshold leakage current when two or more transistors are turned off together [7].

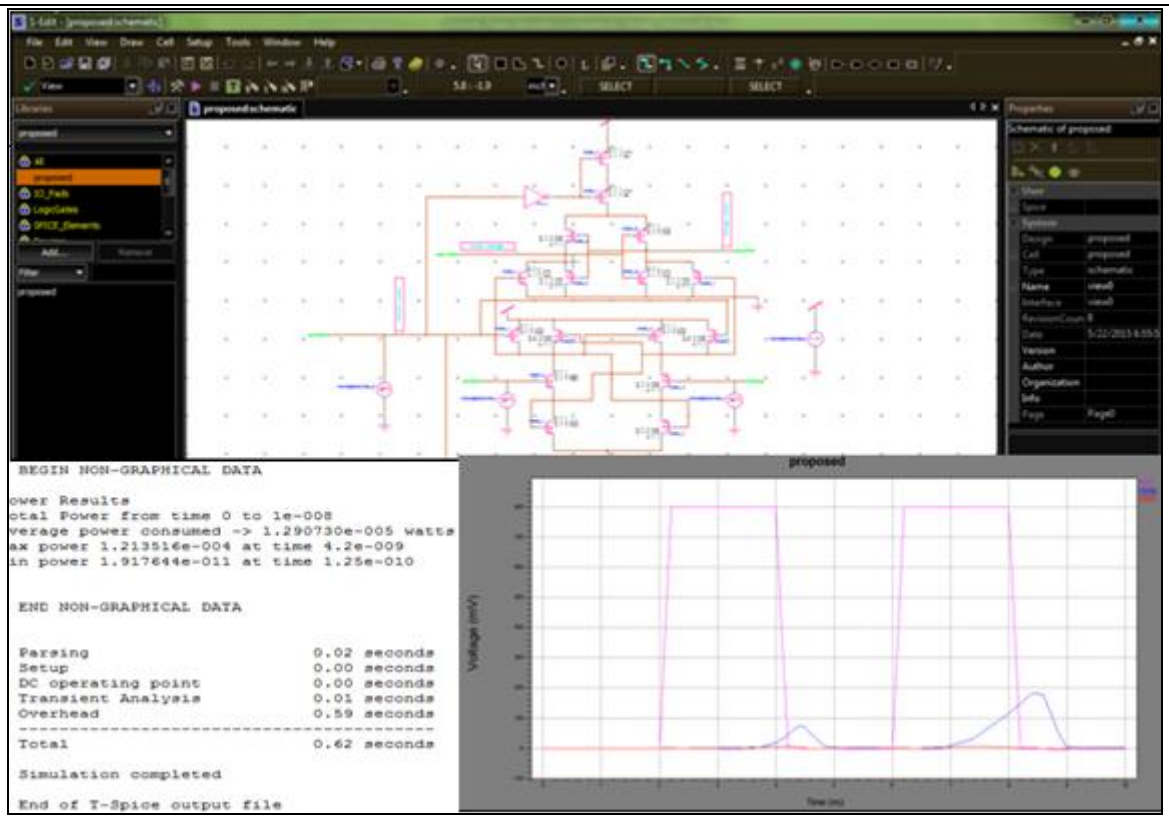

Fig 3: Schematic with simulation result of Proposed Double-Tail Comparator with Stack Technique.

3.3 Using Sleepy-Stack Technique

This is the one of the other technique under sleep methods; the key idea of the sleepy stack technique is to combine the sleep transistor approach during active mode with the stack approach during sleep mode. The schematic with simulation result of the double-tail comparator with sleepy stack technique is shown in Fig 4 [7]. The sleepy stack technique divides existing transistors into two transistors each typically with the same width W1 half the size of the original single transistor's width W2. Then sleep transistor is added to one of the transistors in each set of two stacked transistors.

The activity of the sleep transistors in sleepy stack is same as the activity of the sleep transistors in the sleep transistor technique. The sleep transistors turned on during active mode and turned off during sleep mode. Sleepy stack structure achieves ultra low leakage power consumption during sleep mode while retaining the exact logic state. But the main drawback of this sleepy stack technique is that it increases area a lot.

4. SIMULATION RESULTS

In order to compare the proposed comparator with the conventional double-tail comparator, all circuit have been simulated in a 250nm Tanner EDA technology with Vdd = 0.8v. Table.1 describes the values of power consumed by each comparator designs and those designs after implemented in SAR application.

We can observe from the table that the power consumption obtained by the proposed double-tail comparator is reducing.

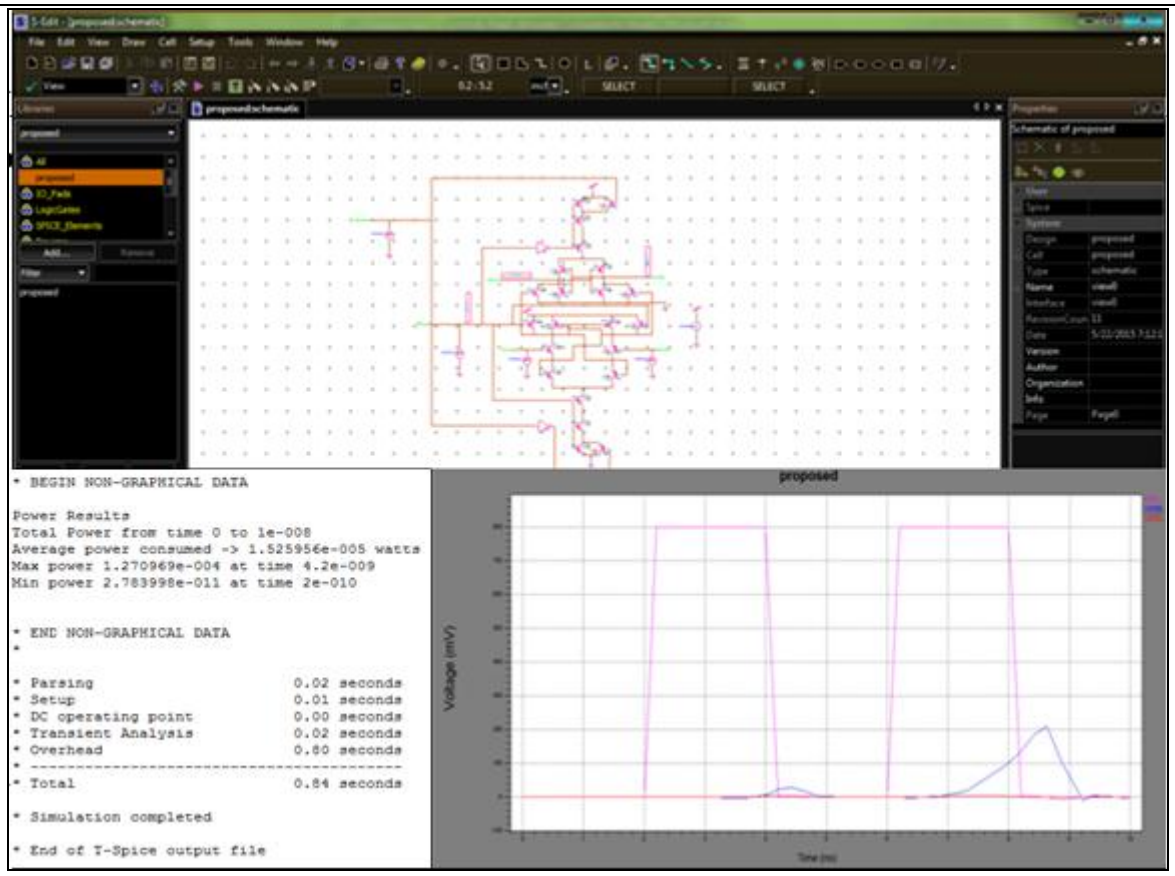

Fig 4: Schematic with simulation result of Proposed Double-Tail Comparator with Stack Technique.

Comparators	Power Consumed in Watts	Improvement in % compared to Existing
Existing Double – Tail Comparator	2.02E-05	-
Proposed Double – Tail Comparator Using Sleep Transistor Technique	1.78E-05	12
Proposed Double – Tail Comparator Using Stack Technique	1.29E-05	36
Proposed Double – Tail Comparator Using Sleepy-Stack Technique	1.53E-05	24

Table 1: Comparison table of power consumed in each comparators.

5. CONCLUSION

The power reduction is calculated using tanner EDA in 250nm technology for various circuits such as conventional double tail dynamic comparator and proposed double-tail comparator with sleep methods. All these circuits are tested separately. Simulation results infer that power reduction is high in all the proposed dynamic comparators with sleep methods.

Kindly say that in this project a comparison of popular existing dynamic comparators with new proposed comparators with sleep methods has been discussed and i can conclude that proposed comparator with stack approach was found to be the best.

6. FUTURE WORK

A successive approximation ADC is a type of analog to digital converter that converts continuous signal to digital value via a binary search through all possible quantization levels before converging upon a digital output for each conversion. Comparing to other ADC's architecture SAR ADC is limited in speed, medium at accuracy, hence to attain the high speed and good accuracy level proposed comparator is implemented within it. The comparator design is replaced with the proposed dynamic comparator to obtain low power consumption and improving the performance of the ADC.

ACKNOWLEDGEMENTS

I convey my gratitude to Asst.Prof Mrs Ashwini N C, Department of Electronics and Communication Engineering, for having constantly monitored the development of the project and guiding me in the right direction. I am grateful to The Head of the department Prof Dr. Sreeramareddy G M, HOD, Department of Electronics and Communication Engineering, for his excellent encouragement in the successful completion of the project.

REFERENCES

1. B. Goll and H. Zimmermann, "*A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65*", *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 11, pp. 810–814, Nov. 2009.
2. S. U. Ay, "*A sub-1 volt 10-bit supply boosted SAR ADC design in standard CMOS*," Int. J. Analog Integr. Circuits Signal Process., vol. 66, no. 2, pp. 213–221, Feb. 2011.
3. A. Mesgarani, M. N. Alam, F. Z. Nelson, and S. U. Ay, "*Supply boosting technique for designing very low-voltage mixed-signal circuits in standard CMOS*", in Proc. IEEE Int. Midwest Symp. Circuits Syst. Dig. Tech. Papers, Aug. 2010, pp. 893–896.
4. B. J. Blalock, "*Body-driving as a Low-Voltage Analog Design Technique for CMOS technology*", in Proc. IEEE Southwest Symp. Mixed-Signal Design, Feb. 2000, pp. 113–118.
5. M. Maymandi-Nejad and M. Sachdev, "*1-bit quantiser with rail to rail input range for sub-1V_ modulators*" IEEE Electron. Lett., vol. 39, no. 12, pp. 894–895, Jan. 2003.
6. Y. Okaniwa, H. Tamura, M. Kibune, D. Yamazaki, T.-S. Cheung, J. Ogawa, N. Tzartzanis, W. W. Walker, and T. Kuroda, "*A 40Gb/ s CMOS clocked comparator with bandwidth modulation technique*", IEEE J. Solid-State Circuits, vol. 40, no. 8, pp. 1680–1687, Aug. 2005.
7. Pushpa Saini, Rajesh Mehra," *Leakage Power Reduction in CMOS VLSI Circuits*," International Journal of Computer Applications Volume 55 –No.8, October 2012.
8. Samaneh Babayan-Mashhadi, and Reza Loth, "*Analysis and Design of a Low Voltage Low Power Double Tail Comparator*", vol. 22. No. 2, February 2014.
9. Kaushik Roy, Saibal Mukhopadhyay, Hamid Mahmoodi-Meimand "*Leakage Current Mechanisms and Leakage Reduction Techniques in Deep Submicrometer CMOS Circuits*", Proceedings of the IEEE, vol. 91, No. 2, February 2003.